Amendments to the Claims:

Please cancel Claims 14-20.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original): A method for constructing a semiconductor device, the method comprising:

forming a trench isolation structure and an active region proximate an outer surface of a semiconductor layer;

depositing an epitaxial layer outwardly from the trench isolation structure;

growing a first insulator layer outwardly from the epitaxial layer;

growing a second insulator layer outwardly from the first insulator layer;

forming a gate stack outwardly from the epitaxial layer, the gate stack comprising a portion of the first insulator layer, a portion of the second insulator layer, and a gate formed proximate the second insulator layer, the gate having a narrow region and a wide region; and

heating the epitaxial layer to a temperature sufficient to allow for the epitaxial layer to form a source/drain implant region in the active region.

Claim 2 (original): The method of Claim 1, wherein the trench isolation structure comprises silicon dioxide.

Claim 3 (original): The method of Claim 1, wherein the epitaxial layer has a thickness of approximately 1,000 angstroms to 3,000 angstroms.

Claim 4 (original): The method of Claim 1, wherein the epitaxial layer comprises silicon.

Claim 5 (original): The method of Claim 1, wherein the epitaxial layer comprises silicon germanium.

Claim 6 (original): The method of Claim 1, wherein the epitaxial layer comprises silicon germanium carbon.

Claim 7 (original): The method of Claim 1, wherein the first insulator layer comprises silicon dioxide.

Claim 8 (original): The method of Claim 1, wherein the second insulator layer comprises silicon nitride.

Claim 9 (original): The method of Claim 1, wherein the gate stack comprises a third insulator layer formed outwardly from the second insulator layer, the third insulator layer comprising silicon dioxide.

Claim 10 (original): The method of Claim 1, wherein forming the gate stack comprises:

etching the second insulator layer;
etching the first insulator layer to form a gate region;
growing a gate insulator layer outwardly from the gate region; and
forming the gate outwardly from the gate insulator layer.

Claim 11 (original): The method of Claim 1, wherein forming the gate stack comprises:

etching the second insulator layer using a dry etching process;
etching the first insulator layer using a wet etching process to form a gate region;
growing a gate insulator layer outwardly from the gate region; and
forming the gate outwardly from the gate insulator layer.

Claim 12 (original): The method of Claim 1, wherein:

a length of the narrow region of the gate is approximately one-tenth microns to two microns; and

a width of the narrow region of the gate is approximately 25 microns to 100 microns.

Claim 13 (original): The method of Claim 1, wherein a length of the wide region of the gate is approximately two-tenths microns to two microns greater than a length of the narrow region of the gate.

Claims 14-20 (canceled)